In the Claims:

1. (Original) A content addressable memory (CAM) device, comprising:

CAM logic that is configured to pass an instruction received at an instruction input port to an instruction output port without inspection or alteration so that the CAM device may be operated within a cascaded chain of CAM devices that collectively form multiple databases within a lookup engine.

2. (Original) The CAM device of Claim 1, wherein said CAM logic comprises:

an input instruction register that is configured to latch the instruction received at the instruction input port; and

an output instruction register that is configured to latch the instruction received from the input instruction register.

3. (Original) The CAM device of Claim 2, wherein said CAM logic further comprises an instruction FIFO that is configured to buffer instructions received from the input instruction register.

4. (Original) An integrated circuit system, comprising:

a cascaded chain of CAM devices that is configured to support passing of instructions down the cascaded chain without inspection or alteration using a distributed control architecture.

5. (Original) The system of Claim 4, wherein the CAM devices in said cascaded chain are arranged in a high-to-low CAM priority sequence.

6. (Original) The system of Claim 4, wherein each of the CAM devices in said cascaded chain comprises:

an instruction input port that is configured to receive an instruction from a first instruction cascade interface bus during a first cycle of an instruction operation; and

an instruction output port that is configured to reproduce the instruction on a second instruction cascade interface bus during a second cycle of the instruction operation that is delayed relative to the first cycle.

7. (Original) The system of Claim 5, wherein each of the CAM devices in said cascaded chain comprises:

an instruction input port that is configured to receive a learn instruction from a first instruction cascade interface bus during a first cycle of an instruction operation; and

an instruction output port that is configured to reproduce the learn instruction on a second instruction cascade interface bus during a second cycle of the instruction operation that is delayed relative to the first cycle.

8. (Original) The system of Claim 4, wherein each of the CAM devices in said cascaded chain comprises:

an instruction input port that is configured to receive an instruction from a first instruction cascade interface bus, in-sync with a first cycle of a clock signal generated internal to the respective CAM device; and

an instruction output port that is configured to reproduce the instruction on a second instruction cascade interface bus, in-sync with a second cycle of the clock signal that is delayed relative to the first cycle of the clock signal.

9. (Original) A content addressable memory (CAM) device, comprising:

an instruction input port that is configured to receive an instruction from a first instruction cascade interface bus, in-sync with a first clock signal generated internal to the CAM device; and

an instruction output port that is configured to reproduce the instruction without inspection or alteration on a second instruction cascade interface bus, in-sync with a second clock signal generated internal to the CAM device.

10. (Original) The CAM device of Claim 9, wherein said instruction input port comprises an input register that is responsive to the first clock signal; and wherein said instruction output port comprises an output register that is responsive to the second clock signal.

11. (Original) The CAM device of Claim 10, further comprising an instruction FIFO that is electrically coupled to received instructions from the input register.

Claim 12 (Canceled).

13. (Previously presented) A method of operating a cascaded chain of CAM devices arranged in a high-to-low priority sequence, comprising the step of:

performing a learn operation in the cascaded chain of CAM devices by passing a learn instruction through a plurality of CAM devices in the cascaded chain, without inspection or alteration, using a distributed control architecture that offsets timing of learn operations within each of the plurality of CAM devices.

14. (Previously presented) The method of Claim 13, wherein each of the plurality of CAM devices includes a next free address (NFA) table; and wherein said performing step further comprises the step of:

writing a search key into a CAM core within a selected one of the plurality of CAM devices, in response to evaluating whether an NFA table in the selected one of the plurality of CAM devices has a valid NFA address for the search key.

15. (Previously presented) The method of Claim 14, wherein said performing step further comprises evaluating each of the NFA tables in the plurality of CAM devices to determine whether a valid NFA address for the search key is present.

16. (Original) The method of Claim 15, wherein the step of evaluating each of the NFA tables in the plurality of CAM devices is performed as a sequential operation that follows the high-to-low priority sequence.

17. (Original) The method of Claim 16, wherein the search key is associated with a CAM core database; and wherein said writing step is followed by the step of searching each of the plurality of CAM devices to identify an address of a highest priority invalid entry within the CAM core database.

18. (Original) The method of Claim 17, wherein said step of searching each of the plurality of CAM devices to identify an address is followed by the step of writing the address into the NFA table.

19. (Original) The method of Claim 14, wherein the search key is associated with a CAM core database; and wherein said writing step is followed by the step of searching each of the plurality of CAM devices to identify an address of a highest priority invalid entry within the CAM core database.

20. (Original) The method of Claim 19, wherein said step of searching each of the plurality of CAM devices to identify an address is followed by the step of writing the address into the NFA table.

21. (Original) A method of operating a cascaded chain of CAM devices, comprising the step of:

performing a learn operation in the cascaded chain of CAM devices by:

writing a search key associated with a database into a selected one of the cascaded chain of CAM devices, in response to evaluating whether an NFA table in the selected one of the cascaded chain of CAM devices has a valid NFA address for the search key; and

searching each of the CAM devices in the cascaded chain to identify an address of a highest priority invalid entry in a CAM device that retains the at least a portion of the database.

22. (Original) A content addressable memory (CAM) device, comprising:

CAM logic that is configured to pass a learn instruction received at an instruction input port to an instruction output port without inspection or alteration and with at least one cycle of latency.

23. (Original) The CAM device of Claim 22, wherein said CAM logic comprises:

an input instruction register that is configured to latch the learn instruction received at the instruction input port; and

an output instruction register that is configured to latch the learn instruction received from the input instruction register.

24. (Original) The CAM device of Claim 23, wherein said CAM logic further comprises an instruction FIFO that is configured to buffer learn instructions received from the input instruction register.